AMO UWB Module

(SR040 with embedded antenna)

Rev 0.9

(ASMOP1CO0A1)

Revision	Contents	Date
0.1	New	7th, September, 2020.
0.9	Revision	23th, June, 2021

23th, June, 2021

AMOSENSE Co., LTD.

Notes

The contents of this data sheet are subject to change without notice. Please confirm the specifications and delivery conditions when placing your order.

Table Of Contents

1. Introduction

The UWB module is based on NXP's SR040 Ultra Wideband (UWB) transceiver IC. It integrates all RF circuitry, power management and clock circuitry in one module compliant to IEEE 802.15.4 HRP UWB PHY.

It can be used for 2-way ranging measurement and TDoA based one way ranging.

Embedded PHY and MAC compatible with FiRa consortium specification.

1.1 Key Features

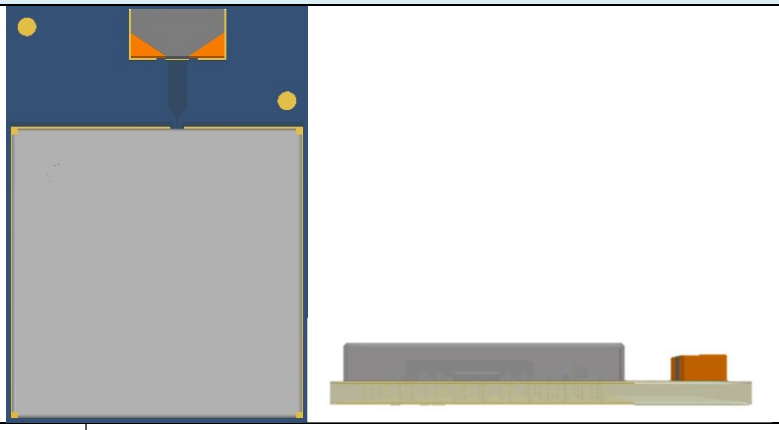
AMO UWB SR040 Module with embedded antenna	
	
ANT Type	• Internal Antenna
Size	• 13mm x 18 mm x 2.7mm
Interface	• SPI(Host)
Main ICs	• SR040, ARM® Cortex-M33 32 Bit processor (SR040 comes with onboard flash to accommodate fixed FW.)
Reference Clocks	• 55.2MHz clock
Frequency Band	• 6.24 GHz ~ 8.24 GHz
Supply Voltage	• 1.8 to 3.6 (Typ. 3.3) V
Output Power	• MAX +12 dBm
Package	• Metal Shield CAN

Table 1. Key Features

* Shield CAN size : 12.25mm x 12.25mm x 1.65mm

1.2 Applications

① IOT application

② UWB Trackers

③ UWB Tags

2. Part Numbering

[Example]

Device Family

AS MO P 1C O 0 A 1

Company name

AS = AMOSENSE

Device type

MO = Module, **DT** = Tag, **DA** = Anchor

Type

P = PCB, **F** = FPCB, **K** = Package

Chipset

1B = SR150, **1C** = SR040

Configuration

O = UWB Only, **B** = UWB + BLE(MCU), **M** = UWB + MCU

MCU Part number

0 = UWB Only, **1** = QN9090

Antenna

N = Non, **A** = Antenna, **R** = Receptacle, **S** = SMA

Version

1

Note : Provisional designation

3. Module Block Diagram

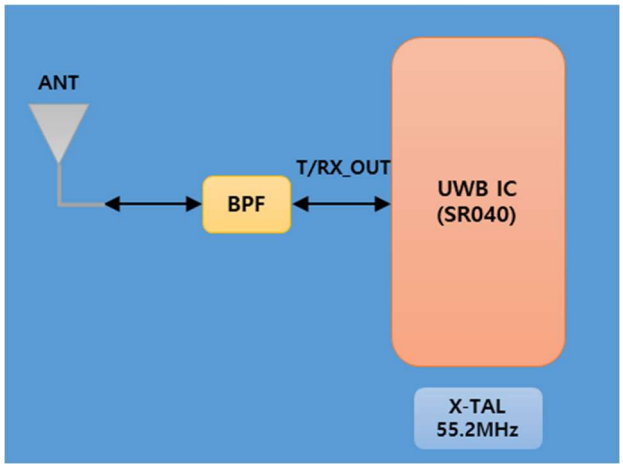


Figure 1. Block Diagram of AMO UWB Module

4. Module Characteristics

4.1 Electrical Characteristics

Parameter	Min	Typ.	Max	Unit
Supply Voltage(VDD)	1.8	3.3	3.6	V
Operating Temperature	-30	25	+85	˚c
RF Input Power(UWB signal)	-20	-	-	dBm
ESD (Human Body Model)			2000	V

Table 2. Absolute Maximum Ratings

4.2 RF Characteristics

- T = 25°C, VDD = 3.3 V (typ.)

Parameter	Condition	Min	Typ.	Max	Unit
Frequency Range		6.24	-	8.24	GHz
TX Output Power	Programmable transmitter output power	-	12	-	dBm
RF Sensitivity	6.8 Mbps Data rate	-	-	-92	dBm
Supply Current	Hard Power Down State (HPD)	-	500	-	nA
	DPD State retention mode	-	550	-	uA
	DPD without state retention	-	5	-	uA
	Active State, CPU running	-	5.1	-	mA
Current Consumption	Active State RX	-	131		mA
	Active State TX 12dBm	-	115		mA
	SR040 is dedicates to battery operated UWB devices, embedded PMU enable operation from a coin cell battery				

* Current limiter : Configurable current limit from 5 mA to 20 mA, in steps of 1 mA

Table 3. RF Characteristics

5. Power management

5.1 Power supply states

SR040 supports following power states.

System power state	Description
Reset	Default state when chip boots up. Active state is entered from this state.
Active	The device is running in normal active mode and chip can perform TX and RX
Deep power down mode (DPD)	The device is in low power state. The memory is not supplied and wake up timer is not running. Wake up is possible through external interrupt. No RF communication is possible in this state.
DPD retention mode	The device is in deep power down state, but the memory is supplied and wake up timer is running.
Hard power down mode	The device is powered down. It can be activated by the chip reset.

Table 4. System power states description

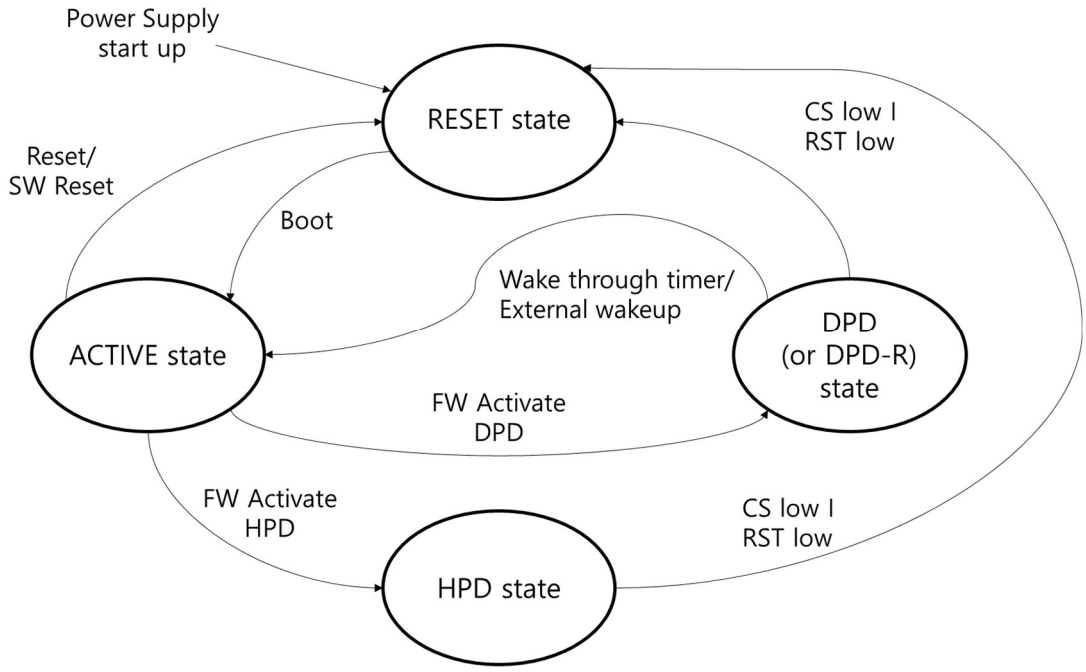


Figure 2. SR040 power modes state diagram

6. SPI Host Interface

A single serial peripheral interface (SPI) block is provided. It supports the following key features.

- SPI data rate up to 10 MHz supported
- Master and slave operation, but default configuration is slave operation
- Data transmissions of 1 to 16 bit supported directly. Larger frames supported by software
- The SPI building block supports separate transmit and receive FIFO buffers with 8 entries each with 16-bit width
- Data can be transmitted to a slave without the need to read incoming data
- The device supports wake-up from power-saving modes through events on the SPI interface

Pin	functionality	Description
P17 / SCLK	SCK	Serial Clock for SPI. SCK is a clock signal used to synchronize the transfer of data. It is driven by the master and received by the slave. When the SPI interface is used, the clock is programmable to be active high or active-low. SCK only switches during a data transfer. It is driven whenever the Master bit in CFG equals 1, regardless of the state of the Enable bit.
P21 / SDI	MOSI	Data input when SPI is a slave in 4-wire operation, it clocks in serial data from this signal.
P20 / SDIO	MISO	Data input when SPI is a master in 4-wire operation, it clocks in serial data from this signal.
P14 / CS_N	SSEL0	Slave Select 0 for SPI. By default, this signal is active low but can be selected to operate as active high. When the SPI is a slave, any SSEL in an active state indicates that this slave is being addressed. The SSEL pin is driven.

Table 5. SPI Pin description

In addition to the 4-wire mode, two additional and optional control lines are provided (resulting in the 6-wire mode).
These are the RDY_N (Ready not) and the INT_N(Interrupt not).
The RDY_N signal handshakes the CS_N (generated from the host) in order to ensure that the SPI transfer will be successful. CS_N can be understood as a request to send (RTS) and the RDY_N as clear to send (CTS). Using the RDY_N signal is optional, and the host can always rely on waiting some predefined time to transmit a command or read a response. The RDY_N signal is activated (active low) always after CS_N activation and deactivated after CS_N deactivation. When the host (SPI master) accidentally transmits a command while the RDY_N is not activated, the SR040 will ignore the transfer.
The purpose of the INT_N signal is to inform the host that there are data to be read from the device, or an event has occurred which needs to be inspected by the host.

Using the INT_N signal is optional, and the host can always rely on polling the SR040 for its status and act accordingly. The INT_N signal is active low. It can be activated at any time, because events that trigger the INT_N are asynchronous and cannot be foreseen. The INT_N is active as long as a pending event isn't read out. INT_N is cleared after the SPI transmission was started by the host activating CS_N and the SR040 handshaking this by activating RDY_N. If another event is pending, INT_N is reactivated.
SPI interfaces typically allow configuration of clock phase and polarity. These are referred as numbered SPI modes, as described in Table 6 and Figure 3. CPOL and CPHA are configured by internal CFG register. CPHA refers to the Clock Phase option and CPOL refers to the Clock Polarity.

CPOL	CPHA	SPI Mode	Description	SCK Rest state	SCK data change edge	SCK data sample edge
0	0	0	The SPI captures serial data on the first clock transition of the transfer (when the clock changes away from the rest state). Data is changed on the following edge.	Low	Falling	Rising
0	1	1	The SPI changes serial data on the first clock transition of the transfer (when the clock changes away from the rest state). Data is captured on the following edge.	Low	Rising	Falling
1	0	2	Same as mode 0 with SCK inverted.	High	Rising	Falling
1	1	3	Same as mode 0 with SCK inverted.	High	Falling	Rising

Table 6. SPI mode summary

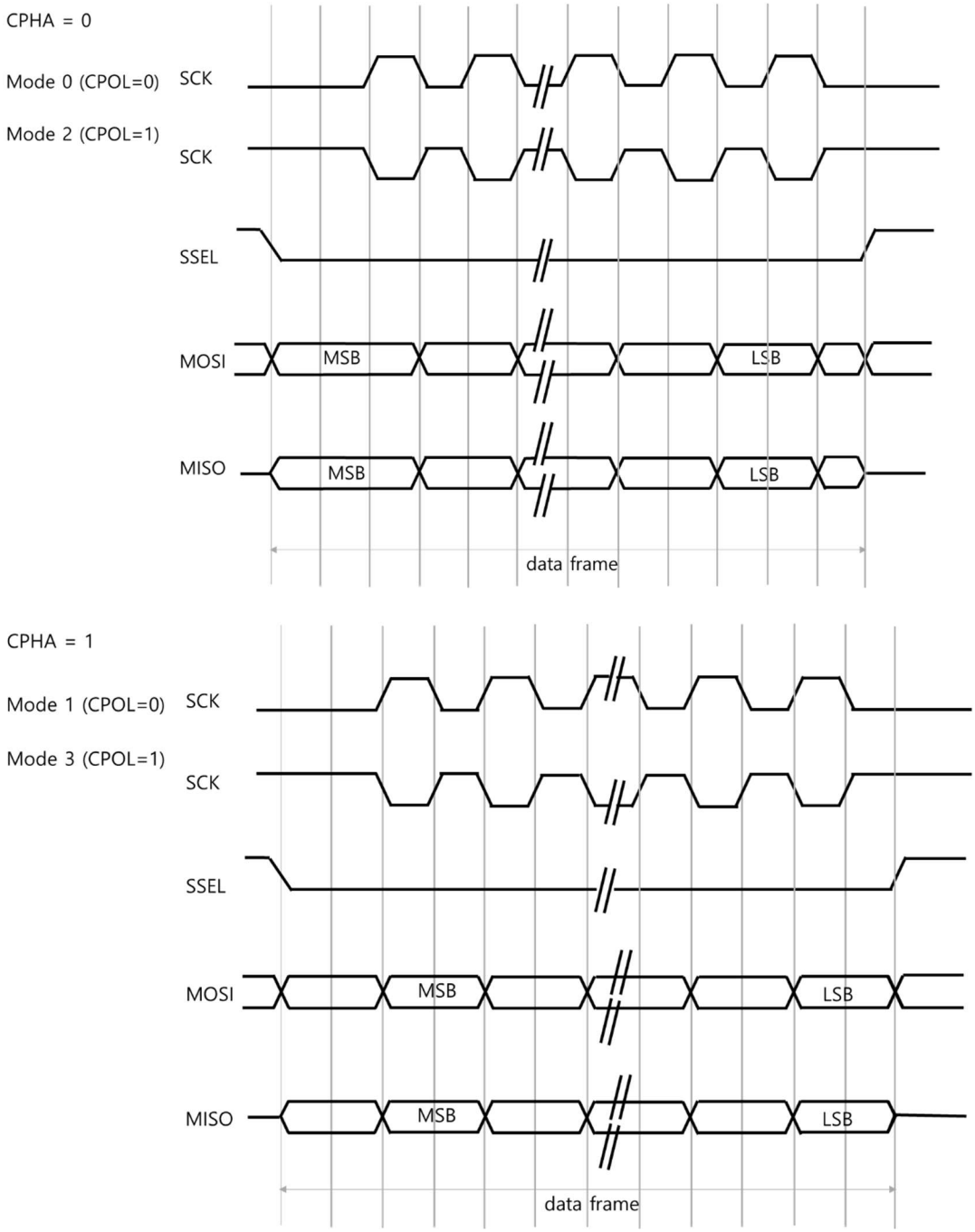


Figure 3. SPI date frame

7. Current limiter in UWB SR040 module

The current limiter is intended for applications with coin cell battery supply, to maximize the lifetime of the battery. It minimizes battery stress by limiting the maximal current drawn by the IC. The current limit is configurable by SW. Figure 4 shows how the current limiter is connected in the application.

The current limiter comprises from 5 mA to 20 mA, in steps of 1 mA.

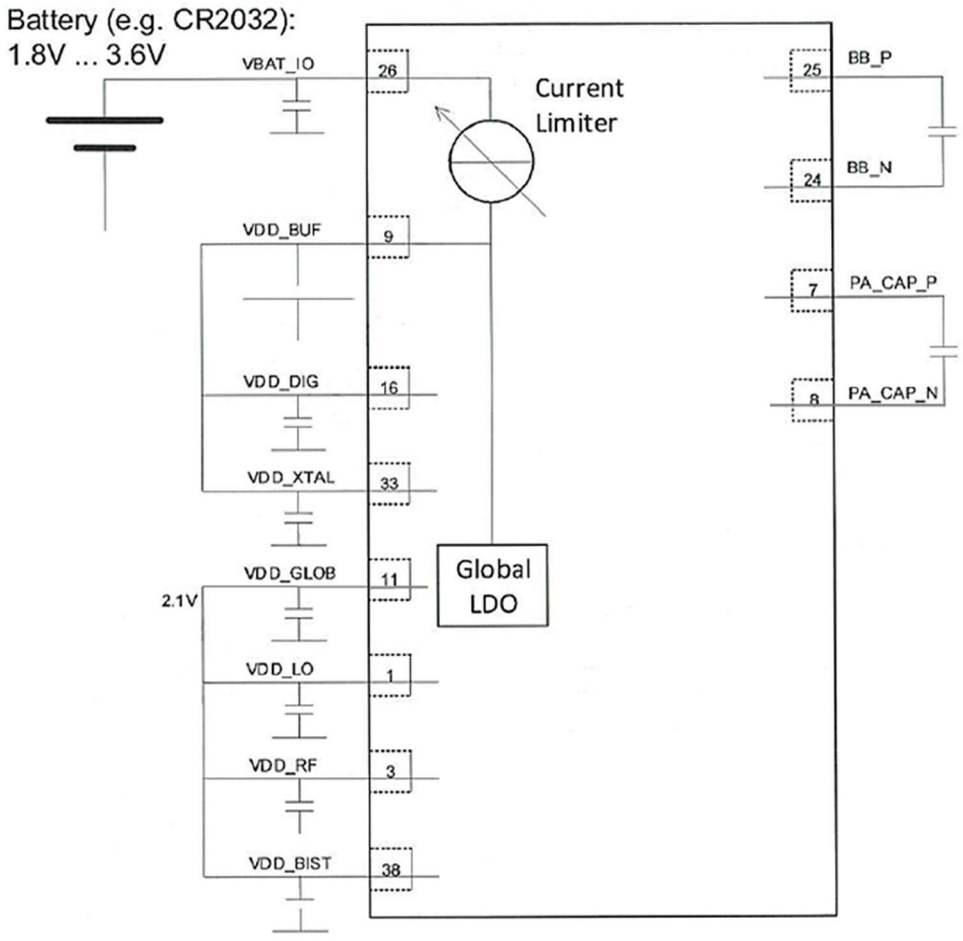


Figure 4. Current limiter in UWB SR040 module

8. UWB Antenna

No	Item	Spec.	Remark
1	Frequency Range [MHz]	6000 ~ 8000	
2	VSWR	Max 2.0:1	
3	Polarization	Linear	
4	Impedance [Ω]	Nominal 50	

Table 7. UWB Antenna Electrical Specifications

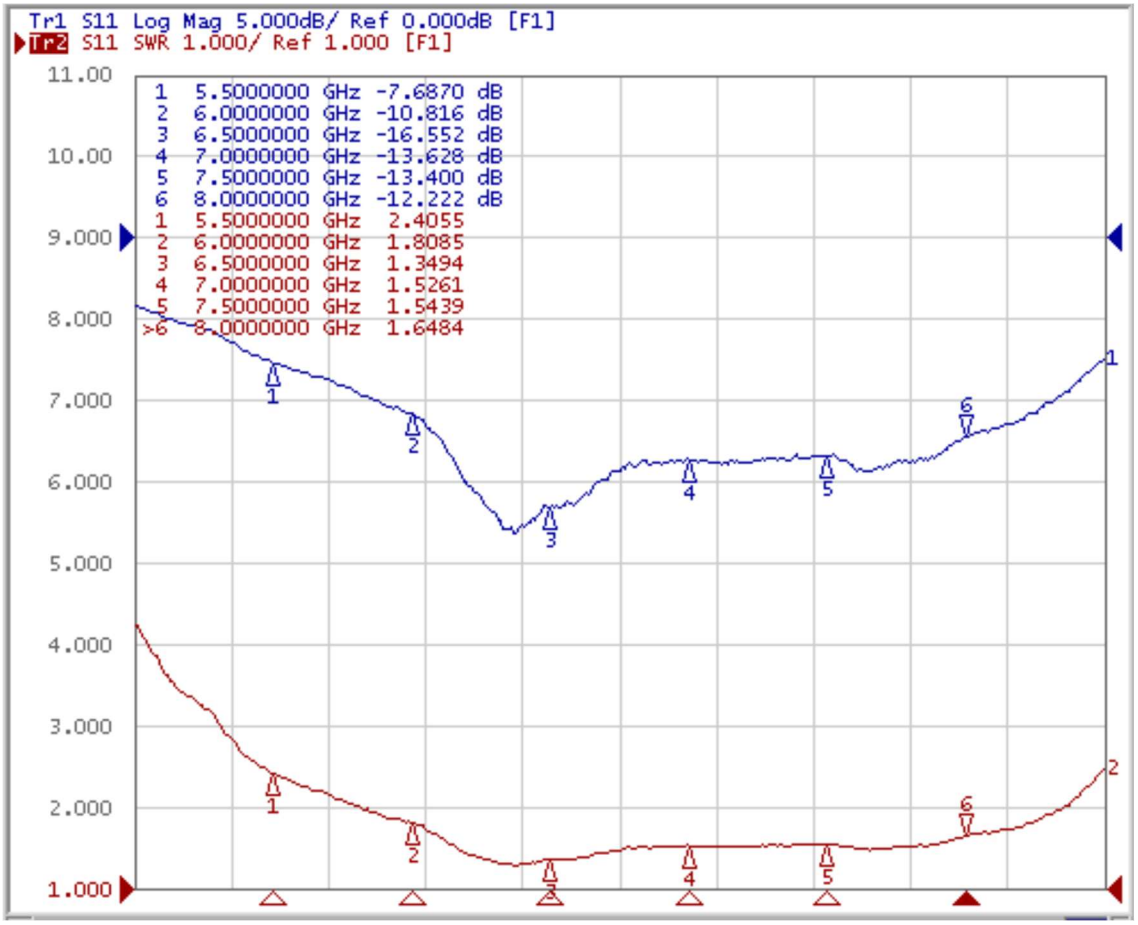
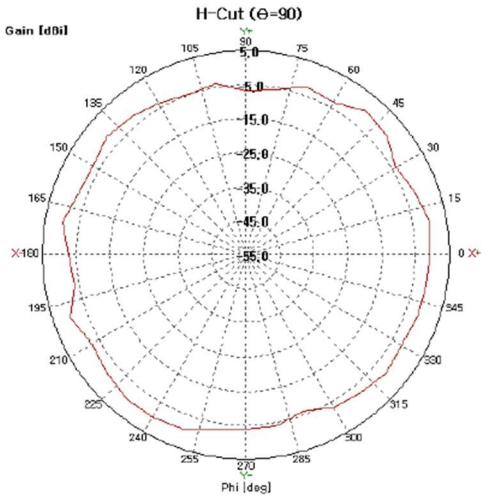


Figure 5 : Typical Measurement Result (VSWR & Return-loss)

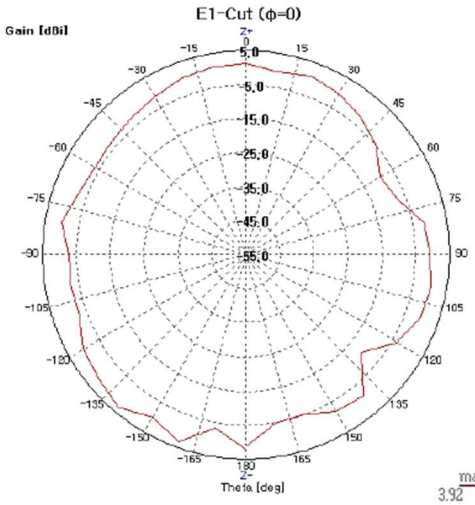
Freq. [MHz]	Peak Gain [dBi]	Avg. Gain [dBi]	Efficiency [%]
6000	4.50	-1.49	70.9
6500	4.14	-0.94	80.6
7000	3.86	-0.87	81.7
7500	4.90	-1.25	75.0
8000	4.28	-0.82	82.8

Table 8. UWB Antenna Measured Radiation Characteristics

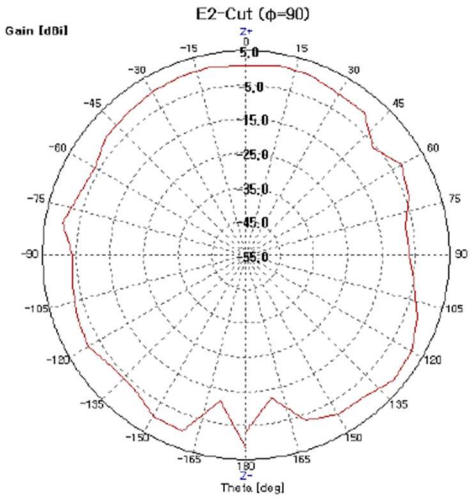
H-Cut (θ=90)

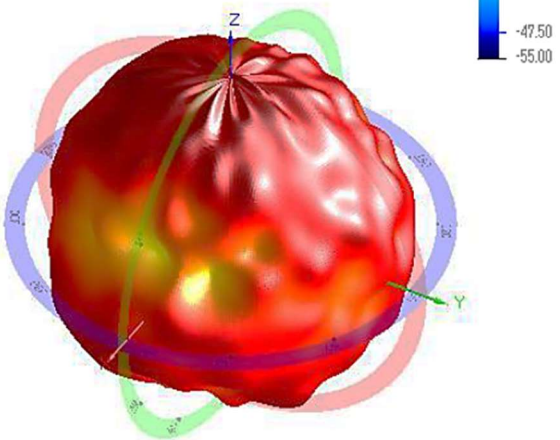


E1-Cut (φ=0)



E2-Cut (φ=90)





9. Application design-in information

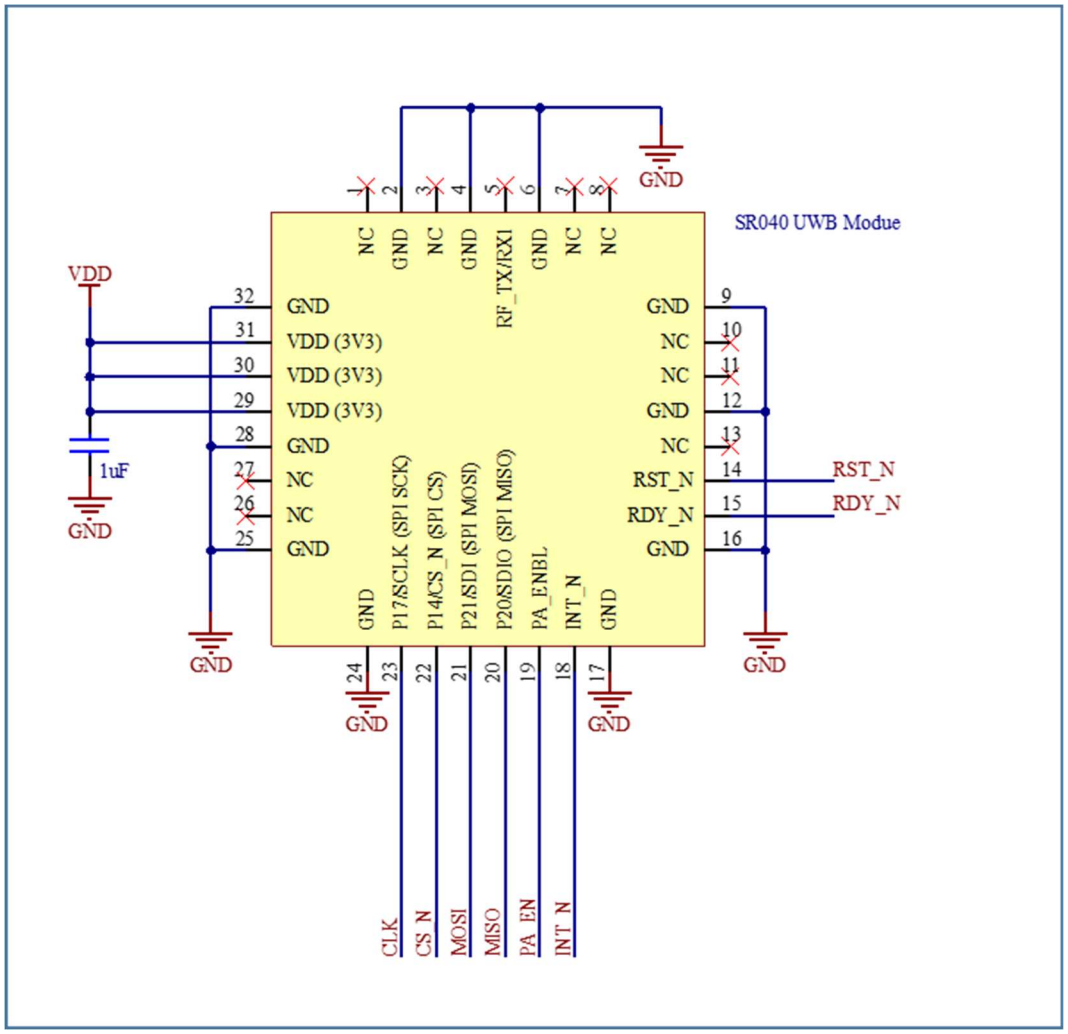


Figure 6. UWB SR150 Module Reference Circuit

10. Module Package

10.1 Pinout Description

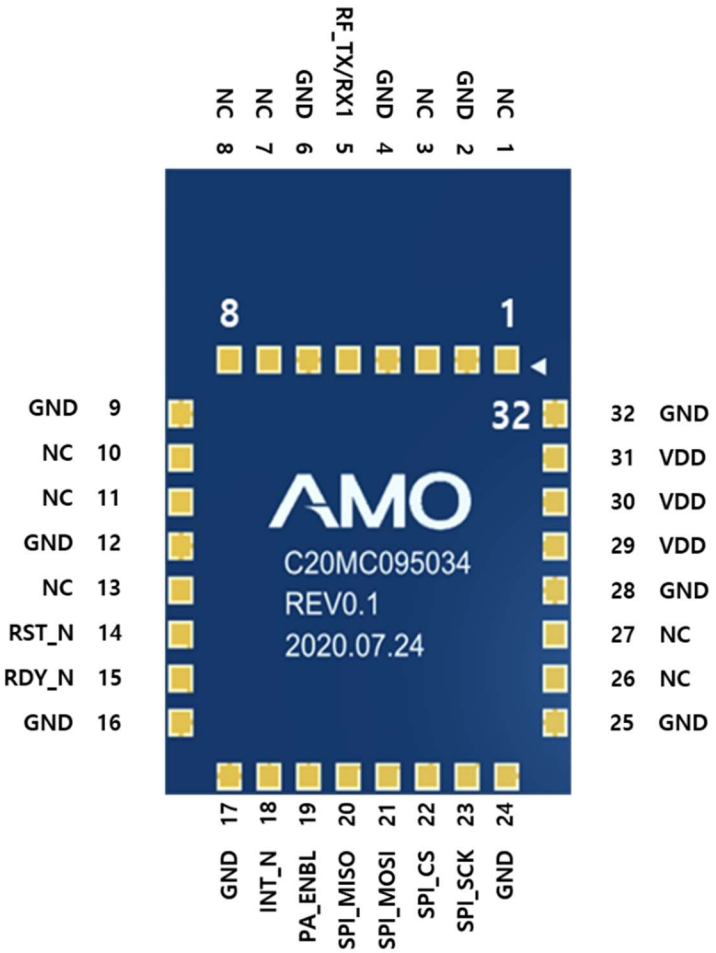


Figure 7. Pinout Description(Bottom View)

10.2 Pin Description Box

PIN	PIN Name	PIN Type	Description
P1	NC		
P2	GND	G	Ground supply
P3	NC		
P4	GND	G	Ground supply
P5	RF_TX/RX1	RF	TX/RX
P6	GND	G	Ground supply
P7	NC		
P8	NC		
P9	GND	G	Ground supply
P10	NC		
P11	NC		
P12	GND	G	Ground supply
P13	NC		
P14	RST_N	I	Reset input
P15	RDY_N	I/O	Ready output
P16	GND	G	Ground supply
P17	GND	G	Ground supply
P18	INT_N	I/O	Interrupt output
P19	PA_ENBL	I/O	Gating signal for an optional external PA
P20	SPI_MISO	I/O	MISO connection for the SPI host interface
P21	SPI_MOSI	I/O	MOSI connection for the SPI host interface
P22	SPI_CS	I/O	Slave select connection for the SPI host interface
P23	SPI_SCK	I/O	clock for the SPI host interface
P24	GND	G	Ground supply
P25	GND	G	Ground supply
P26	NC	P	
P27	NC	I/O	
P28	GND	G	Ground supply
P29	VDD	P	3.3V Power supply
P30	VDD	P	3.3V Power supply
P31	VDD	P	3.3V Power supply
P32	GND	G	Ground supply

Table 9. Pin Description

10.3 Module Dimension or Footprint

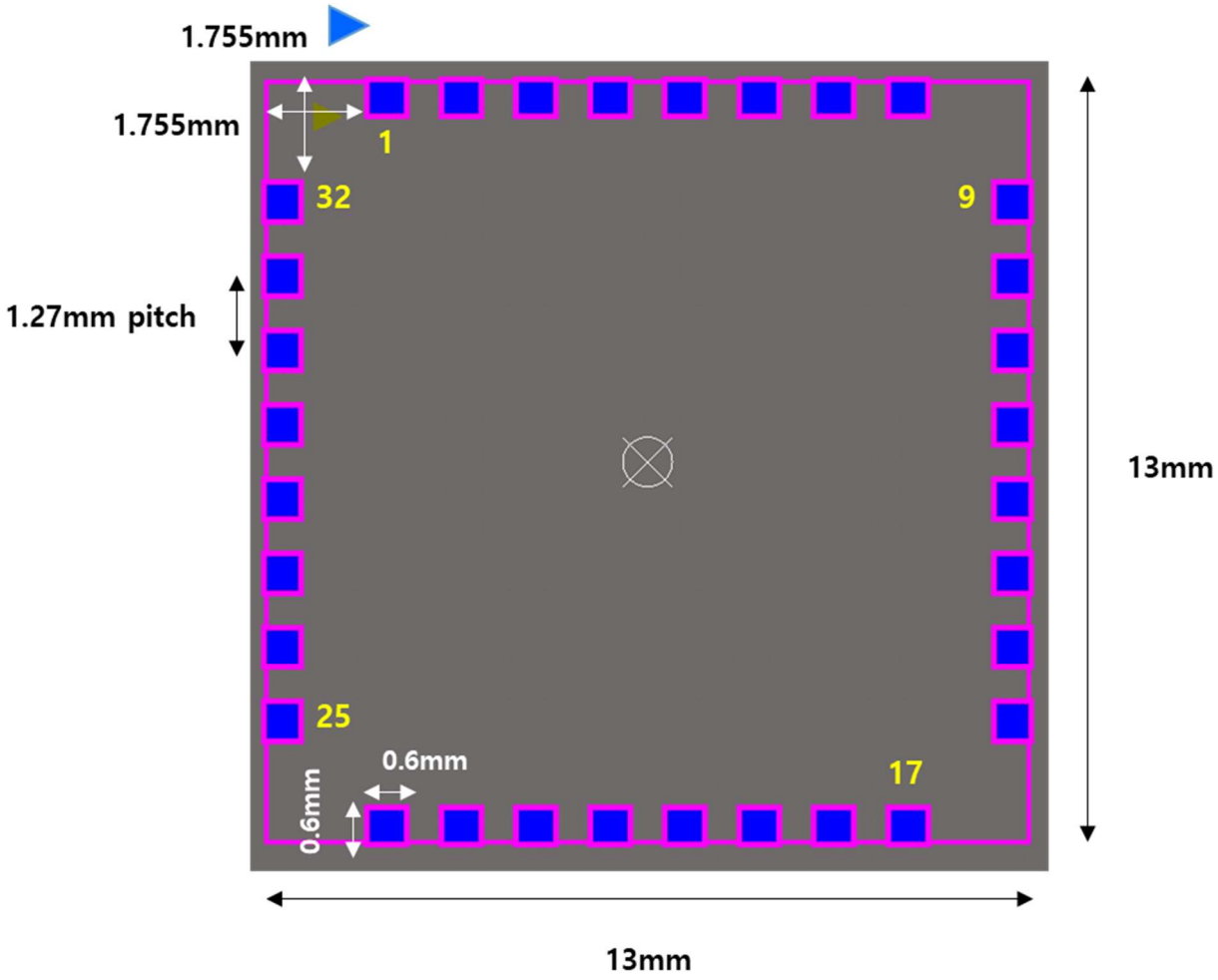


Figure 8. Pin Dimension or Footprint (TOP View)

11. Packing

Description	Data
Module Dimension	13mm*18mm*2.7mm
Reel Carrier Pocket	32W*20P
Reel Cover Tape	25.5mm*480m
Module Quantity	1K

Table 10. Reel Packing Description

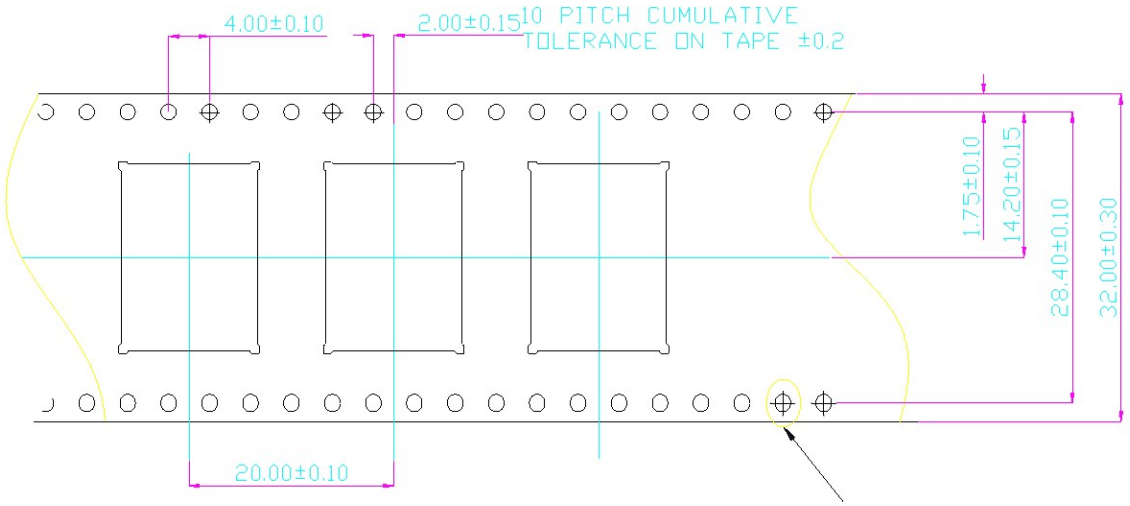


Figure 9. Reel Packing

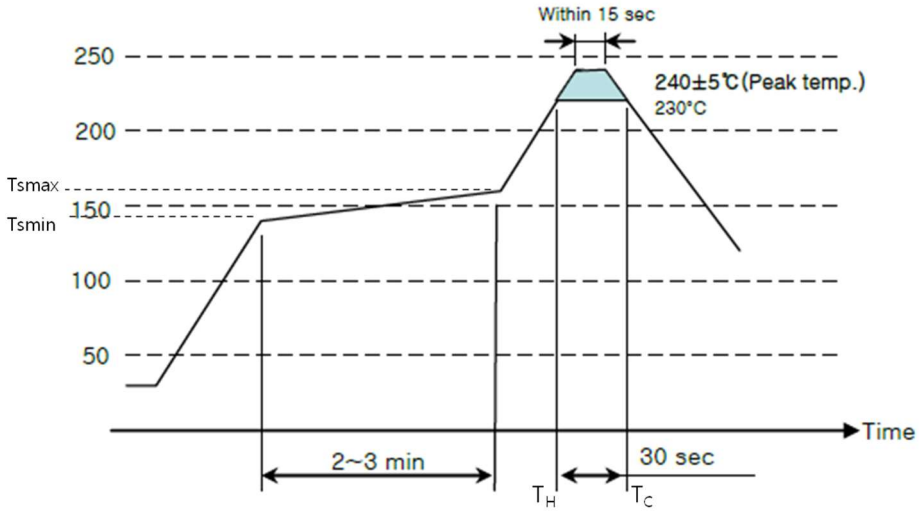
12. Soldering Condition

12.1 Manual Soldering – Pb Free

① Soldering Temperature: 360℃ ± 5℃, 5sec max.
(Solder : Sn /Ag /Cu : 96.5 /3.0 /0.5)

② Moisture sensitivity precautions, as indicated on the packing, must be respected at all times

12.2 Recommended Reflow Condition – Pb Free



Profile Feature	Pb-Free Assembly
Preheat -Temperature Min (T_{smin}) -Temperature Typical ($T_{stypical}$) -Temperature Max (T_{smax}) -Time T_{smin} to T_{smax}	 -140˚C -150˚C -160˚C -2 ~ 3 min
Peak Temperature	240±5˚C
Time of actual peak temperature	Max. 15 seconds

Heating to Cool	
-Temperature Heating (T_H)	-230˚C
-Temperature Cool (T_C)	-230˚C
-Time T_H to T_C	-30 seconds

13. Glossary

Abbreviation	Long term
BPF	Band Pass Filter
DPD	Deep Power Down
HPD	Hard Power Down
HRP	High Rate Pulse Repetition Frequency
NC	Not Connected
OTP	One Time Programmable
PMU	Power Management Unit
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
RTLS	Real-time locating systems
RX	Receiver
SFD	Start of Frame Delimiter
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
STS	Secure Training Sequence
SWD	Serial Wire Debug
TDoA	Time Difference Of Arrival
ToF	Time of Flight
TX	Transmitter
UART	Universal Asynchronous Receiver and Transmitter